REMRARK

Claims 1-8 are pending of which claims 1, 5, 7 and 8 have been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter adds by way of amendments made to claims or otherwise to the application. For at least the foregoing reason, Applicants respectfully submit that claims 1-8 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of objection to Specification

1. The disclosure is objected because of the following informalities: the specific atio n is replete with grammatical errors to mentio n specifically.

In response thereto, enclosed please find an amended versio n of the specific atio n in which all grammatical errors are corrected.

2. *Claims 1-8 is objected because of the following informalities: in claim 1 it appears that "decayed" should actually be -delayed-. On lin e 3 in the claim 1, "a main output stage" should be changed to- the main output stage-.*

In response thereto, applicants explains why a term of "a decayed signal" is used, instead of "a delayed signal", through the specificatio n. Referring to Fig.2, the node V_{c2} is configured in the same manner of reference to the ground as V_{c4}. As a result, a

current flows out from theV_{g2}, while another current from the positive terminal of V2 flows into the V_{g2}; in other words, V_{g2} is connected in reverse-polarity. Therefore, V2 decays the V_{g2} so as to be unable to turn on the transistor 214 in an assistant output stage. That is, a magnitude of V_{g4} differs that of V_{g2} by a voltage V2 so that Vg4 is described a decayed signal, instead of delayed signal, which is usually referred to a signal with an invariant magnitude and a time delay. Therefore, applicants consider the term "a decayed signal" is proper.

In addition, claims 1, 5, 7 and 8 are amended as instructed by the examiner so as to there is no any informality in these claims

Discussion for objection to claims under 35U.S.C. 102(e)

Claim 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.6,784,719 (Okamoto, hereinafter referred to Okamoto)

As to claim 1 note Fig.7, where the recited "main outputstage"reads on circuit 2 (the "main current"is the current through either inverter I1 or inverter I2);the cited "monitoring stage"reads on the series-connected FETs N2 and N3 (the recited "deplayed push/pull signals read on the pull/up/down currents output provided by FETs N2 and N3, respectively); and the recited "assistant output stage"reads on inverter I5 (its

output currents are provided to the node between inverter I2 and inverter I3)

In response thereto, applicants do not agree the above examiner's allegation and provide the following arguments.

The invention motives and functionalities of Okamoto are to control a duty of output signals because of duty of signals being changed when passing a level shift circuit, which is totally distinct from "enhancing a slew rate," the invention motives and functionalities of the present invention. Furthermore, to more clarify the feature of the present invention, the claim 1 is amended as follows.

1. (currently amended) A circuit for enhancing a slew rate by providing an assistant current to a main output stage having a main current, comprising:

a monitoring stage for receiving a signal from a the main output stage and outputting a decayed push signal and a decayed pull signal; and

an assistant output stage for receiving the decayed push signal and the decayed pull signal to output an assistant current[[.]], whereby the slew rate can be enhanced by adding the assistant current to the main current.

Obviously, Okamoto fails to teach, suggest or disclose "whereby the slew rate can be enhanced by adding the assistant current to the main current." as claimed and featured in the amended claim 1.The amended claim 1 is patentable over

Okamoto under35 U.S.C. 102(e).

With respect to claims 2-4, no matter whether they are conventional, they are patentable over Okamoto as a matter of law, for at least the reason that they contain their base independent claim 1's features.

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.6,777,986 (Hidaka, hereinafter referred to Hidaka)

As to claims 1,2 , note Fig.3, where the recited "main output stage" reads on the push-pull of FETs 1a and 2a; the recited "monitoring stage" reads on the combination of delay 12b and gates 13b,14b; and the recited "assistant output stage" reads on the push-pull of FETs 1b,2b.

As to claims 5,6, note Fig.80A, where the detecting of the first and second inputs occurs due to the action of differential amplifier 490; the push/pull currents are through the FETs 492 and 494, respectively; the feedback of thee push/pull currents (claim 6)is from the common drain of the FETs 492 and 494 to the non-inverting input of amplifier 490.

In response thereto, applicants do not agree the above examiner's allegation and provide the following arguments.

The reference number and device symbols of 1a, 2a,1b and 2b in Fig.3 in Hidaka can not be regarded as a push-pull circuit as disclosed in the present invention because these devices are

also not described in the description of Fig.3 in the specification. Since the push-pull circuit is constructed through a series-connected complement type of FETs. However, from the Fig.3, 1a, 2a,1b and 2b are obviously not complement type of FETs. As a result, circuit shown in Fig.3 in Hidaka fails to output a push or a pull signals. Most importantly, Hidaka fails to teach, suggest or disclose "whereby the slew rate can be enhanced by adding the assistant current to the main current." as claimed and featured in the amended claim 1. The amended claim 1 is patentable over Okamoto under35 U.S.C. 102(e).

Invention motives of the Hidaka is to solve a output unstable problem of a DRAM, which is caused by passing a large current through a parasite inductance generated by pads, In addition, a circuit shown in Fig.80A is a voltage regulator and functions to provide a voltage VccQ with NMOS transistors 1 and 2 of a circuit 926.A PMOS 492 is able to push a lager current to a load terminal while a NMOS 494 functions as a constant current source (when ψck is high) and constitutes a negative feedback(from the non-inverting terminal of 490 through c1, then VccQ and finally to the non-inverting terminal of 490). As a result, VccQ has the same voltage as VREFa. In other words the function of the circuit shown in Fig.80A is different from that of the present invention.

In addition, in Fig. 80A, the reference number 492 is PMOS FET while the reference number 494 is NMOS FET. However,

only the gate of the PMOS FET with the reference number 492 is connected to an output of OP 490 so that the reference number 492 and 494 FETs can not function as a push/pull circuit. In other words, Hidaka fails to teach, suggest or disclose" generating a push current when a voltage of the second input is larger than a voltage of the first input and is enough to turn on at least one of the switches; and generating a pull current when a voltage of the first input is larger than a voltage of the second input and is high enough to turn on at least one of a plurality of switches." as claimed and featured in claim 5. Hence, claim 5 is patentable over Hidaka.

With respect to claims 6,7 and 8, no matter whether they are conventional, they are patentable over Hidaka as a matter of law, for at least the reason that they contain their base independent claim 5's features.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-8 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-8 and the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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